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BOX PATENT APPLICATION
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Dear Sir:

Transmitted herewith for filing is the patent application of:

Inventor: Shuichi Matsuda
For: Semiconductor Device

Enclosed are the following:

[ ] Letter: SUBMISSION OF INCOMPLETE APPLICATION
[X] Specification 10 pages; Claims 4 pages; Abstract 1 page
[X] Declaration and Power of Attorney
[X] sheet(s) of drawings 3 pages
[X] An assignment of the invention to: NEC Corporation
[ ] A verified statement to establish small entity status
[X] A certified copy of Japanese application No. 359478/1997, filed December 26, 1997
[ ] Prior Art Disclosure Statement
[ ] Preliminary Amendment

Priority is hereby claimed under 35 USC 119 by way of Japanese patent application No. 359478/1997 filed December 26, 1997.

Benefit is hereby claimed under Title 35, United States Code 119(e) of United States provisional application No. _____ filed _____.

The filing fee has been calculated as shown below:

		SMALL ENTITY	LARGE ENTITY
BASIC FEE:		$ 395.00	$ 790.00
TOTAL CLAIMS:	20 - 20 = -0-	x 11 =	x 22 = -0-
INDEPENDENT CLAIMS:	4 - 3 = 1	x 41 =	x 82 = 82.00
MULT. DEPEND. CLAIMS:		+ 135 =	+ 270 = -0-
TOTAL:		$	$ 872.00

[X] A check in the amount of $ 912.00 is enclosed to cover the fees.
[X] ($40.00 Assignment recordal fee is included)

The Commissioner is hereby authorized to charge any additional filing fees required under 37 CFR 1.16 or credit any overpayment to Deposit Account No. 08-1391.

Attorney of Record
Norman P. Soloway, Reg. No. 24,315

CERTIFICATE OF EXPRESS MAILING

"Express Mail" Mailing Label No. EM155447728US Date of Deposit December 28, 1998

I hereby certify that this paper and the papers listed thereon are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, and is addressed to BOX PATENT APPLICATION, Commissioner of Patents, US Patent and Trademark Office, Incoming Mailroom, 1B01 Crystal Plaza 2, 2021 Jefferson Davis Highway, Arlington, VA 22202-3602.

Signature of person mailing: Kristine Stevens
Name of person mailing: Kristine Stevens

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention :

This invention relates to a semiconductor device and more particularly to a semiconductor device in which any fault connection between chip electrodes and a wiring on a wiring substrate is prevented.

2. Description of the Related Art :

There is currently known a semiconductor device called chip side package (hereinafter called the CSP) whose size is reduced almost to the size of a semiconductor ship.

The conventional CSPs are separated into a number of groups according to the kind of an interposer for mounting the semiconductor chip. This interposer is exemplified by a film carrier.

However, if the wiring on the film carrier and the chip electrodes on the semiconductor chip are interconnected by pressing under heat, such joint tends to be separated due to possible stresses so that the joint would become electrically opened.

Fig. 7 of the accompanying drawings of the present specification is a perspective view showing a conventional ordinary-type CSP.

As shown in Fig. 7, a semiconductor chip 1 is disposed on a TAB (Tape Automated Bonding) tape 2, which is a film carrier, has a size substantially equal to that of the TAB tape 2.

Aluminum (Al) chip electrodes (not shown) of the semiconductor chip 1 are electrically connected with bumps 9 via non-illustrated bumps

in through-holes of the TAB tape 2. The whole of the semiconductor chip 1 is sealed by sealing resin 8 such as epoxy resin.

Fig. 8 is a fragmentary, enlarged cross-sectional view taken along line VIII-VIII of Fig. 7.

In Fig. 8, the TAB tape 2 is composed of a polyimide tape 2b , which is to be a base, and a wiring 2a of copper foil formed on the polyimide tape 2b, serving as a film carrier (a wiring substrate) on which the semiconductor chip 1 is to be supported.

The wiring 2a is previous formed on the polyimide tape 2b in a desired wiring pattern by vapor deposition of copper in the through-holes of the polyimide tape 2b. On the exposed surfaces of each bump 6, another bump 5 as of nickel (Ni) or gold (Au) is formed by plating.

The chip electrodes 4 are electrically connected with a wiring layer 3 in the semiconductor chip 1, the surface of which is covered with a chip covering film 12 so as to expose the chip electrodes 4.

The thus fabricated film carrier is used in assembling the semiconductor package as follows:

Firstly, with the bumps 5 aligned in confronting relationship with the chip electrodes 4, the wiring 2a are pressed against the bumps 6 under heat or ultrasonic waves using bonding tools. As a result, the individual bump 5 deforms to form gold-aluminum (Au•Al) alloy at the contact surface so that the bump 5 and the corresponding chip electrode 4 are pressed against each other under heat. Then the semiconductor chip 1 and chip covering film 12 are attached to each other by an adhesive material 11 to complete the semiconductor package. In the meantime, a solder resist 10 is applied over the surface of the exposed wiring 2a for corrosion-proofing.

However, according to this conventional technology, after the bump 5 and the chip electrode 4 are interconnected as pressed under

heat, their joint tends to be separated due to possible stress as of the TAB tape 2, and as a result, the separated joint will be found as a fault connection during inspection after assembling of the semiconductor package.

SUMMARY OF THE INVENTION

With the foregoing problems in view, it is an object of this invention to provide a semiconductor device free of any connection fault between chip electrodes and bumps.

According to a first aspect of the invention, the above object is accomplished by a semiconductor device comprises: a wiring substrate having a predetermined pattern of wiring formed on one surface; a semiconductor chip disposed on the other surface of the wining substrate and having two or more chip electrodes in a common wiring layer; the wiring substrate having a number of through-holes; and a number of bumps formed respectively in the through-holes in confronting relationship with the chip electrodes and electrically connecting the wiring with the chip electrodes.

According to a second aspect of the invention, the above object is accomplished alternative by a semiconductor device comprises: a wiring substrate having a predetermined pattern of wiring formed on one surface; a semiconductor chip disposed on the one surface of the wining substrate and having two or more chip electrodes in a common wiring layer; and a number of bumps disposed on the wiring respectively in confronting relationship with the chip electrodes and electrically connecting the wiring with the chip electrodes.

According to a third aspect of the invention, the above object is accomplished in another alternative way by a semiconductor device

comprises: a TAB (tape automated bonding tape having a predetermined pattern of wiring formed on one surface; a semiconductor chip disposed on the other surface of the TAB tape and having two or more chip electrodes in a common wiring layer; the TAB tape having a number of through-holes; and a number of bumps formed respectively in the through-holes in confronting relationship with the chip electrodes and electrically connecting the wiring with the chip electrodes.

According to a fourth aspect of the invention, the above object is accomplished by still another alternative way by a semiconductor device comprises: a TAB tape having a predetermined pattern of wiring formed on one surface; a semiconductor chip disposed on the one surface of the TAB tape and having two or more chip electrodes in a common wiring layer; and a number of bumps disposed on the wiring respectively in confronting relationship with the chip electrodes and electrically connecting the wiring with the chip electrodes.

In the semiconductor device of any one of the first through fourth aspects of the invention, as a preferred feature, the chip electrodes are arranged from an edge of the semiconductor chip toward its inner side.

As another preferred feature, the chip electrodes are arranged parallel to an edge of the semiconductor chip and the wiring is bent at at least one position.

As still another preferred feature, the chip electrodes are arranged parallel to an edge of the semiconductor chip and the wiring has an end width larger than an inter-electrode distance between the chip electrodes.

As a further preferred feature, the chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of the semiconductor chip.

In the construction of the semiconductor device according to this invention, the device has at least two sets of chip terminals and bumps for a common wiring layer so that if the joint at one position happens to be separated, the remaining joints would be kept from being separated. Accordingly this semiconductor package is free of any connection fault.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings in which :

Fig. 1 is a fragmentary plan view of a semiconductor device according to a first embodiment of this invention;

Figs. 2(a) and 2(b) are fragmentary cross-sectional views taken along line II-II of Fig. 1, showing the process in which the semiconductor device of Fig. 1 is fabricated;

Fig. 3 is a fragmentary cross-sectional view showing a semiconductor package to which the construction of Fig. 1 is applied;

Fig. 4 is a fragmentary plan view showing a semiconductor device according to a second embodiment of the invention;

Fig. 5 is a fragmentary plan view showing a semiconductor device according to a third embodiment of the invention;

Fig. 6 is a fragmentary cross-sectional view showing a semiconductor device according to a fourth embodiment of the invention;

Fig. 7 is a perspective view showing a conventional ordinary-type CSP (chip size package); and

Fig. 8 is a fragmentary, enlarged cross-sectional view taken along line VIII-VIII of Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The principles of this invention are particularly useful when applied to a semiconductor device, various preferred embodiments of which will now be described with reference to the accompanying drawings.

Fig. 1 is a fragmentary plan view of a semiconductor device according to a first embodiment of this invention.

In Fig. 1, parts or elements similar to those of Fig. 8 are designated to the same reference numbers. A semiconductor chip 1 is disposed on a TAB (tape automated Bonding) tape 2, which is a film carrier (wiring substrate), has a size substantially equal to that of the TAB tape 2. Two chip electrodes 4 as of aluminum (Al) are connected to a common wiring layer 3 of the semiconductor chip 1.

Each of the chip electrodes 4 of the semiconductor chip 1 is electrically connected with a common wiring 2a on the TAB tape 2, and at one end of the wiring 2a, a pad 2c is formed to which a bump is to be attached. The wiring 2a is formed of copper in a desired pattern on the TAB tape 2.

The fabrication process of the semiconductor device of the first embodiment will now be described with reference to Figs. 2(a) and 2(b).

Fig. 2(a) and 2(b) are cross-sectional views taken along line II-II of Fig. 1, showing the process in which the semiconductor device of Fig. 1 is fabricated.

Firstly, in Fig. 2(a), the TAB tape 2 serving as a film carrier is composed of a polyimide tape 2b, which is to be a base, and a wiring 2a of copper foil formed on the polyimide tape 2b. Then, with the bumps 5 aligned with the chip electrodes 4, the wiring 2a is pressed against the bumps 6 with application of heat or ultrasonic waves by two bonding tools 7. Thus the semiconductor chip 1 is mounted on the TAB tape 2.

As shown in Fig. 2(b), the pressure of the bonding tools 7 deforms the individual bump 5 to form gold-aluminum (Au•Al) alloy at the contact surface, and as a result, the two bumps 5 and the chip electrodes are pressed against each other under heat.

For a stronger joining strength, three or more chip electrodes 4 may be disposed one in corresponding to each set of the bumps 5 and 6.

Fig. 3 is a fragmentary cross-sectional view showing a semiconductor package in which the structure of Fig. 1 is incorporated.

In Fig. 3, the wiring 2a is connected at two positions one to each of the chip electrodes 4 via the respective sets of bumps 5, 6. At one end of the wiring 2a, a pad 2c is formed to which a large bump 9 for connection with a package substrate is mounted.

Figs. 4 and 5 are fragmentary plan views showing second and third embodiment of the invention.

In Figs. 4 and 5, parts or elements similar to those of Fig. 3 are designated by the same reference numbers. In the second and third embodiments, the two chip electrodes 4 connected with one and the same wiring layer 3 are arranged parallel to an edge of the semiconductor chip 1.

In the second embodiment of Fig. 4, a wiring 2a bent (by a right angle) at the other end portion is connected to the two chip electrodes 4. In the third embodiment of Fig. 5, a wiring 2a having an end width larger than the distance of the two chip electrodes 4. Of course, in either case, the wiring 2a and the chip electrodes 4 are interconnected via bumps (not shown).

This invention can applied also to any terminal, such as a power-source terminal (VCC), a ground terminal (GND) and a signal terminal, of the semiconductor chip 1. If it is applied to the ground

terminal, the following results can be obtained.

Namely, in general, a semiconductor chip is equipped with a plurality of power-source terminals and a plurality of ground terminals so that, if connection fault happens to occur at one joint, the other joints remain closed to completely perform its original function. However, if connection fault is found even at one joint during product inspection by the user, he or her might doubt about the technology level and technology level of the manufacturer. Such danger can be avoided by applying this invention to at least power-source and ground terminals. Although, as a demerit, the area occupied by the chip electrodes would increase, possible influence is negligibly small as long as the invention is applied to only power-source terminals and ground terminals. Besides, since sure connection can be achieved, it is valuable to apply the invention to power-source terminals and ground terminals even with some risk of increasing the area the chip electrodes occupy.

In the illustrated embodiments, the bumps 5 are disposed on the rear surface of the semiconductor chip 1. Alternatively, the wiring 2a and the bumps 5 are disposed in confronting relationship with one another as shown in Fig. 6.

According to the semiconductor device of this invention, the wiring on the wiring substrate is connected with two or more chip electrodes connected to a common wiring layer of the semiconductor chip so that, if even a single joint happens to be separated, the other joints remain closed. According the semiconductor device is free of any connection fault as a whole.

It is thus apparent that the present invention is not limited to the above embodiments but may be changed and modified without departing from the scope and spirit of the invention.

Finally, the present application claims the priority of Japanese Patent Application No. Hei9-359478 filed on December 26, 1997, which is herein incorporated by reference.

What is claimed is:

1. A semiconductor device comprises:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wining substrate and having two or more chip electrodes in a common wiring layer;

said wiring substrate having a number of through-holes; and

a number of bumps formed respectively in said through-holes in confronting relationship with said chip electrodes and electrically connecting said wiring with said chip electrodes.

2. A semiconductor device according to claim 1, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side.

3. A semiconductor device according to claim 1, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position.

4. A semiconductor device according to claim 1, wherein said chip electrodes are arranged parallel to an edge of said semiconductor ship and said wiring has an end width larger than an inter-electrode distance between said chip electrodes.

5. A semiconductor device according to claim 1, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

6. A semiconductor device comprises:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wining substrate and having two or more chip electrodes in a common wiring layer; and

a number of bumps disposed on said wiring respectively in confronting relationship with said chip electrodes and electrically connecting said wiring with said chip electrodes.

7. A semiconductor device according to claim 6, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side.

8. A semiconductor device according to claim 6, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position.

9. A semiconductor device according to claim 6, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes.

10. A semiconductor device according to claim 6, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

11. A semiconductor device comprises:

a TAB (tape automated bonding tape having a predetermined pattern

of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having two or more chip electrodes in a common wiring layer;

said TAB tape having a number of through-holes; and

a number of bumps formed respectively in said through-holes in confronting relationship with said chip electrodes and electrically connecting said wiring with said chip electrodes.

12. A semiconductor device according to claim 11, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side.

13. A semiconductor device according to claim 11, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position.

14. A semiconductor device according to claim 11, wherein said chip electrodes are arranged parallel to an edge of said semiconductor ship and said wiring has an end width larger than an inter-electrode distance between said chip electrodes.

15. A semiconductor device according to claim 11, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

16. A semiconductor device comprises:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB

tape and having two or more chip electrodes in a common wiring layer; and

a number of bumps disposed on said wiring respectively in confronting relationship with said chip electrodes and electrically connecting said wiring with said chip electrodes.

17. A semiconductor device according to claim 16, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side.

18. A semiconductor device according to claim 16, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position.

19. A semiconductor device according to claim 16, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes.

20. A semiconductor device according to claim 16, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

ABSTRACT OF THE DISCLOSURE

A semiconductor device equipped with a TAB (tape automated bonding) tape. A desired pattern of wiring is formed on one surface of the TAB tape and a semiconductor chip having tow or more chip electrodes is disposed on the other surface of the TAB tape. The wiring and the chip electrodes are electrically interconnected via bumps that are formed in through-holes of the wiring in confronting relationship with the chip electrodes. This prevents fault connection between the chip electrodes and the bumps.

Fig. 1

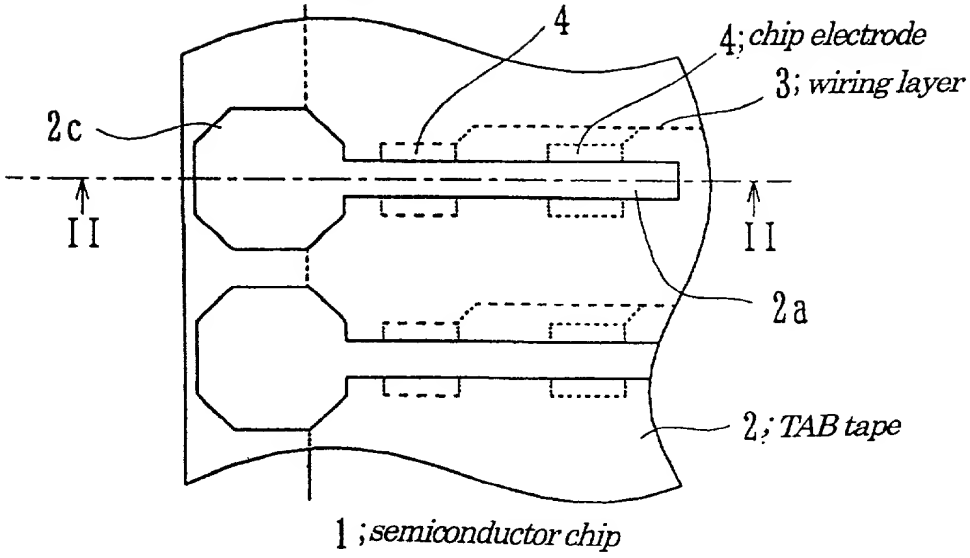


Fig. 2(a)

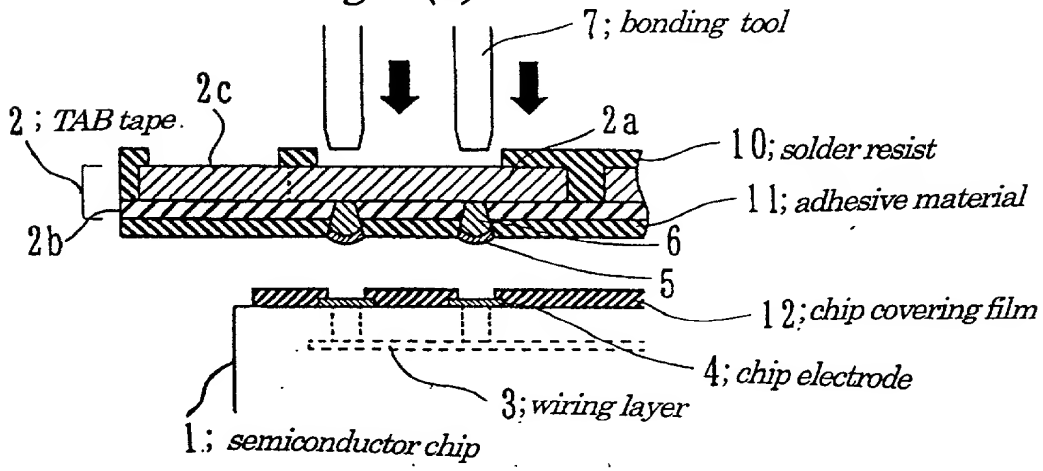
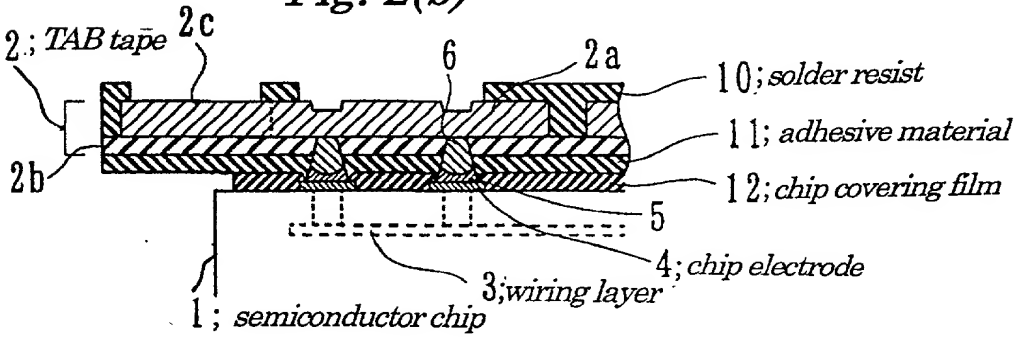


Fig. 2(b)



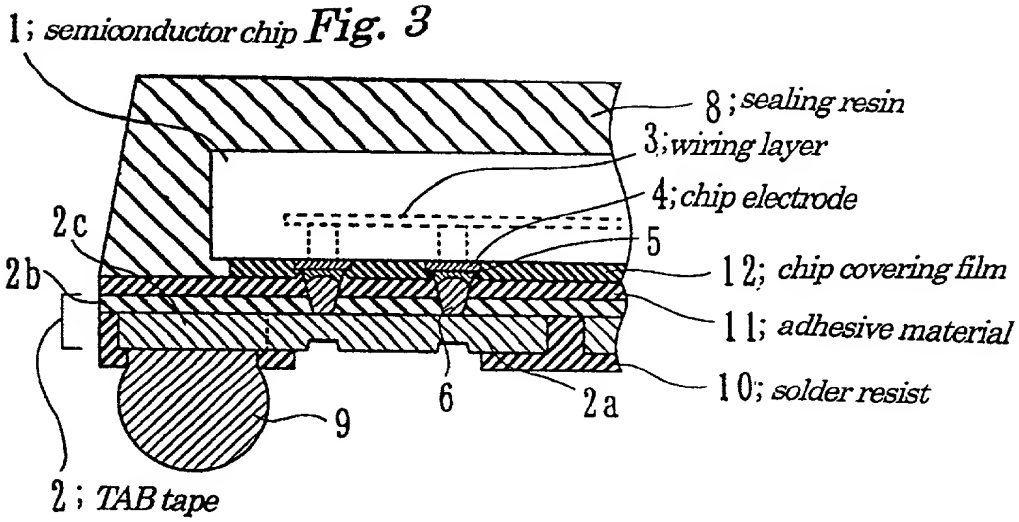


Fig. 3

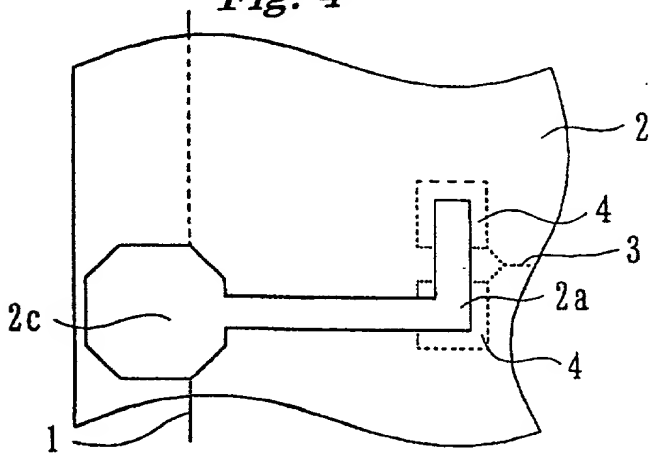


Fig. 4

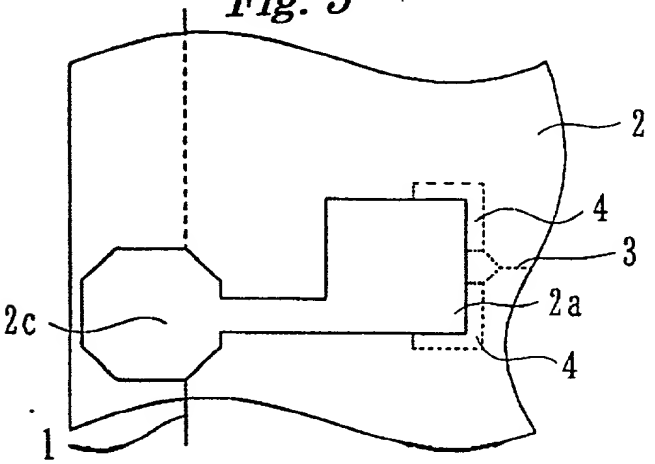


Fig. 5

Fig. 6

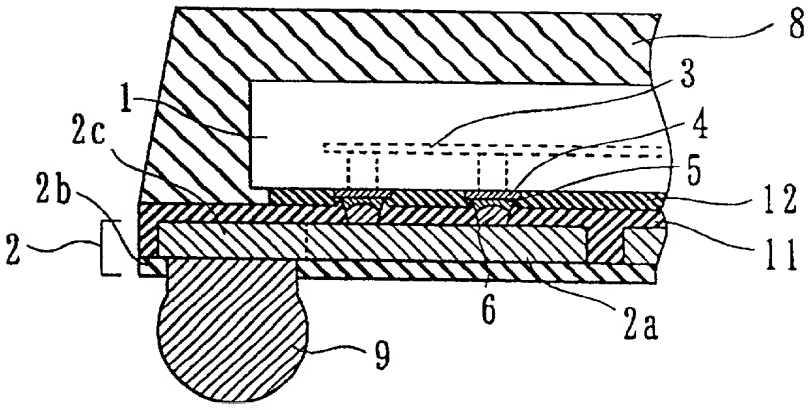


Fig. 7 *(PRIOR ART)*

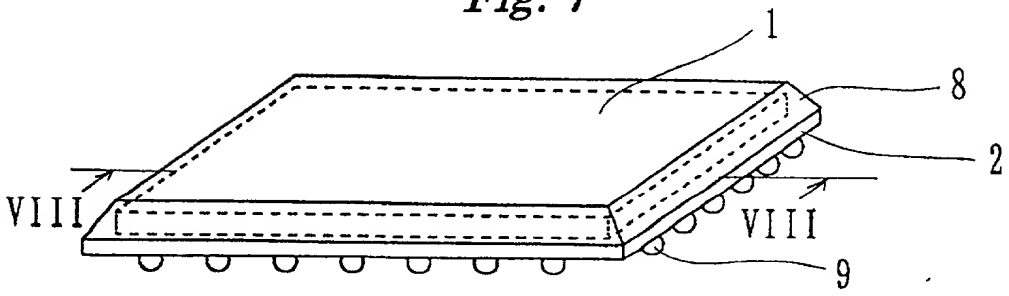
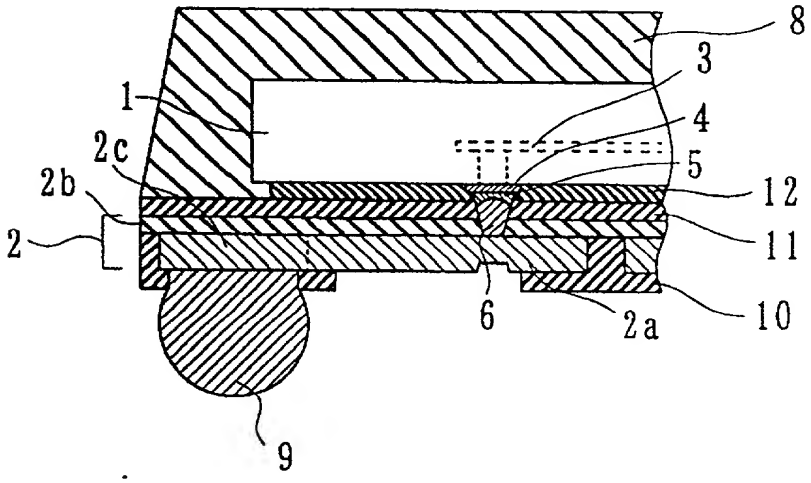


Fig. 8 *(PRIOR ART)*



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket No: NEC N98039

First Named Inventor: SHUICHI MATSUDA

Complete if known: Serial No: _____ Filing Date: December 28, 1998

Group Art Unit: _____ Examiner: _____

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SEMICONDUCTOR DEVICE, the specification of which: ☒ is attached hereto **or** ☐ was filed on _____ as application Serial No. _____, and was amended on _____(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, S. 1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	Certified Copy Attached
359478/1997 (Number)	Japan (Country)	12/26/1997 (Month/Day/Year Filed)	☒ Yes ☐ No	☒ Yes ☐ No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	☐ Yes ☐ No	☐ Yes ☐ No

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below:

Application No: _____ Filing Date: _____

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

US Parent Application or PCT Parent Number	Parent Filing Date	Parent Patent Number (if applicable)

And I hereby appoint HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C., a firm composed of Oliver W. Hayes, Reg. No. 15,867; Norman P. Soloway, Reg. No. 24,315; William 0. Hennessey, Reg. No. 32,032; Susan H. Hage, Reg. No. 29,646; Steven J. Grossman, Reg. No. 35,001; ~~Christopher K. Gagne, Reg. No. 36,142;~~ and Edmund Paul Pfleger, Reg. No. 41,252, or any of them, of 175 Canal Street, Manchester, New Hampshire 03101 (Telephone: 603-668-1400) my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith.

Please direct all future correspondence in connection with this application to the attention of **Norman P. Soloway** HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C., 175 Canal Street, Manchester, New Hampshire 03101 (Telephone: 603-668-1400).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: SHUICHI MATSUDA

First Inventor's signature Shuichi Matsuda Date December 15, 1998
Residence: Tokyo, Japan
Citizenship: Japanese
Post Office Address: c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan

Full name of second joint inventor: _____

Second Inventor's signature _____ Date _____
Residence: _____
Citizenship: _____
Post Office Address: _____